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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,975	CRUTCHFIELD ET AL.	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1 – 5, 10, 11, 16 – 19, 28 - 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5, 9, 10, 14 – 17, 27 – 31, respectively, of copending Application No. 09/895782 in view of the identical recitations of the claims. Examiner notes that there a subtle variations in the claims but believes that the differences are synonymous with the definitions of the original claims.

   This is a provisional obviousness-type double patenting rejection.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because of numerous handwritten captions and labels. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28 - 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Nimishakavi (US Patent 5,594,763).

With regard to claim 28, Nimishakavi teaches a method for initializing a counter to count clock cycles (see Figure 5; count in, Column 3, line 63 – column 4, line 2); detecting a current count value (column 5, lines 7 – 15); defining a sampling count value (column 5, lines 7 – 15); detecting a change in said data (See column 4, line 65 – column 5, line 6); decrementing (provides equivalent functionality as incrementing as discussed further below) said count value if no change in said data is detected (see column 5, lines 7 – 15; examiner notes that reference teaches decrementing count value which provides equivalent functionality for the purposes of counting clock cycles as noted by Nimishakavi (column 6, lines 30 –41)); and, generating a pulse when said counter reaches said sampling count value (see column 5, lines 9-15). Nimishakavi explicitly teaches the counter could be implemented by incrementing the counter (see column 6, lines 30 – 35) as claimed by applicant. It would have been obvious to one of ordinary skill in the art to implement a counter by incrementing as opposed to decrementing based on Nimishakavi's disclosure.

With regard to claim 29, Nimishakavi teaches the method of claim 28 plus the addition of generating step if change in data is detected (See column 4, line 65 – column 5, line 6).

With regard to claim 30, Nimishakavi teaches the method of claim 28 plus the addition of generating step occurs when count value equals sampling count value (column 5, lines 7 – 15).

With regard to claim 31, Nimishakavi teaches the method of claim 28 plus the addition of delaying pulse to center pulse in a data bit (see Column 5, lines 9 – 12, figure 5, d,h,j).

With regard to claim 32, Nimishakavi teaches the method of claim 28 plus the addition of resetting said current count value to zero when said pulse is generated (See column 5, lines 16 - 34). Examiner notes that Nimishakavi describes a count down and restart mechanism, which provides equivalent functionality to that described in claim.

4. Claims 1 – 19, 22 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nimishakavi in view of IEEE P1394b Draft Standard for a High Performance Serial Bus (03/27/2001).

With regard to claim 1, Nimishakavi teaches a method for obtaining a communication link speed (see column 4, lines 33 – 43, where this is interpreted as being inclusive of communication rates), providing a clock signal (see Figure 6, c); providing a counter (see Figure 4, 40); defining (where this is interpreted as being the result of a calculation) a sample count value of counter (see Figure 6, f); decrementing (described in reference as equivalent to incrementing, see column 6, lines 30 –42) counter in relation to clock signal (see column 5, lines 50 – 64, where decrement function of counter is equivalent); determining whether a current count value of counter corresponds to sample count value (see column 5, lines 65 – column 6, line 5), and if current count value corresponds to sample count value then performing a step of generating a synchronous pulse (see column 5, lines 7 – 15), and if current count value does not correspond to sample count value then performing a step of determining whether a signal level of signal has changed (see Figure 4, 46, column 4 line 65

– column 5 line 6). If signal level of data (recovered difference signal) signal has changed then performing a step of ignoring (see column 5, lines 50 – 58) further changes in signal level of data (recovered difference signal) signal until current count value of counter corresponds to sample count value (see column 5, lines 50 – 64) at which time step of generating synchronous pulse is repeated (see column 5, line 65 – column 6, line 5). Nimishakavi is silent on the generation of a difference signal representing a signal level difference between at least two data stream signals. The IEEE 1394b specification defines the use of a differential signal for transmission of data (see page 45, section 4.4.2 2nd paragraph), which could be used as data input to Nimishakavi's invention. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in a USB system to provide to provide a configurable data receiver.

With regard to claim 2, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1 above with Nimishakavi teaching the additional limitation of synchronous pulse is used to signify a time for performing a step of sampling difference signal to extract data from difference signal (See figure 4, RxDPLL ClkOut and column 5, line 65 - column 6, line 5).

With regard to claim 3, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1 above with Nimishakavi teaching the additional limitation of defining a maximum count value of counter, wherein if current count value corresponds to maximum count value then performing a step of resetting counter (See column 5, lines 6- 15, and column 6, lines 30 – 42 where the decrement function is taught to provide equivalent functionality). Examiner notes that Nimishakavi describes a count down and restart mechanism, which provides equivalent functionality.

With regard to claim 4, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1 above with Nimishakavi teaching the additional limitation of checking signal level of

data (where difference) signal each cycle of clock signal (see column 4, lines 28 – 33); storing signal level of data (difference) signal at a first clock cycle as a temporary difference signal (see figure 4, 46); checking signal level of difference signal at a second clock cycle; and comparing signal level of temporary difference signal with signal level of difference signal at second clock cycle (see figure 6, e) where examiner interprets edge detector to be composed of clocked storage elements clocked by DPLL clock. Nimishakavi is silent on the generation of a difference signal representing a signal level difference between at least two data stream signals. The IEEE 1394b specification defines the use of a differential signal for transmission of data (see page 45, section 4.4.2 2nd paragraph), which could be used as data input to Nimishakavi's invention. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in a USB system to provide to provide a configurable data receiver.

With regard to claim 5, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1 above with Nimishakavi teaching the additional limitation of resetting counter (see column 4, line 65 – column 5, line 6); determining whether current count value corresponds to sample count value (see column 5, lines 9 – 15); and if current count value does not correspond to sample count value then performing a step of decrementing (described in reference as equivalent to incrementing, see column 6, lines 30 –42) counter each cycle of clock signal until current count value corresponds to sample count value at which time a step of sampling data (difference) signal to extract data from data (difference) signal is performed (see column 5, lines 16 – 34).

With regard to claim 6, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1. Nimishakavi is silent with respect to communication link with which said communication link speed is associated is an IEEE-1394b bus. Nimishakavi states that his

device is useful for use in serial transmission links (see column 3, lines 24 – 31). IEEE 1394b teaches the use of various speeds for serial communication links. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver.

With regard to claim 7, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1. Nimishakavi is silent with respect to communication link speed being a frequency of one of 98.304 MHz, 196.608 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz. Nimishakavi states that his device is useful for use in serial transmission links (see column 3, lines 24 – 31). IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1). IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver. Examiner notes that 196.608 MHz (S200) does not appear to be a supported electrical interface speed per Table 4-1.

With regard to claim 8, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 1. Nimishakavi is silent with respect to identifying said communication link speed from a plurality of possible communication link speeds. Nimishakavi states that his device is useful for use in serial transmission links (see column 3, lines 24 – 31). IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1), and a means for identifying the communications link speed (see page 52, section 4.7). It would

have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver.

With regard to claim 9, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 8. Nimishakavi is silent with respect to plurality of possible communication link speeds is greater than two. Nimishakavi states that his device is useful for use in serial transmission links (see column 3, lines 24 – 31). IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver.

With regard to claim 10, the limitations of this claim are taught above in claim 1 with the exception of "performing a step of sampling difference (data) signal to extract data from difference (data) signal" which examiner interprets to be equivalent to the limitation of claim 1 of "generating a synchronous pulse" which is used to output sampled data (see column 5, lines 16 –25). The other limitations and motivations are taught above in claim 1.

With regard to claim 11, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 9 above with Nimishakavi teaching the additional limitation of claim 2 above.

With regard to claim 12, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 6 above. Motivation to combine described in claim 6.

With regard to claim 13, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 7 above. Motivation to combine described in claim 7.

With regard to claim 14, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 8 above. Motivation to combine described in claim 8.

With regard to claim 15, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 9 above. Motivation to combine described in claim 9.

With regard to claim 16, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 3 above. Motivation to combine described in claim 3.

With regard to claim 17, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 4 above. Motivation to combine described in claim 4.

With regard to claim 18, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 10 above with the additional limitations taught by claim 5 above. Motivation to combine described in claim 5.

With regard to claim 19, Nimishakavi teaches a device having a synchronous pulse generator having a first data signal input (see Figure 4, RXD which is interpreted as being a recovered differential (difference) signal), a clock signal input (see Figure 4, DPLL Clock), a speed input (Figure 4, Count In) and a synchronous pulse output (see Figure 4, RxDPLL ClkOut where this signal is interpreted as being the same as SPG Out), data signal input being coupled to first output for receiving data signal (see Figure 4, RXD which is interpreted as being a recovered differential (difference) signal), speed signal being adapted to receive a variable representative of communication link speed (see Figure 4, 40, 48) and clock signal input being adapted for receiving a clock signal (see column 4, lines 14 – 20, figure 3, 38),

wherein synchronous pulse generator processes clock signal and data signal to generate a synchronous pulse used for extracting data from data signal (see figure 4, RxD, DPLL Clk, RxD Sync, 40, 52, RxDPLL ClkOut). Nimishakavi is silent on the generation of a difference signal (differential signal) representing a signal level difference between at least two data stream signals. The IEEE 1394b specification defines the use of a differential signal for transmission of data (see page 45, section 4.4.2 2nd paragraph), which could be used as data input to Nimishakavi's invention. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver.

With regard to claim 22, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 19 above with Nimishakavi teaching the additional limitation of synchronous pulse generator includes a speed register (see figure 4, 48 where count register is interpreted to store calculated speed value) for storing a speed value that corresponds with a communication speed of a serial bus.

With regard to claim 23, Nimishakavi in view of IEEE 1394b teaches the limitations of claim 22 above. Nimishakavi is silent with respect to communication link speed is a frequency of one of 98.304 MHz, 196.608 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz. IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver. Examiner notes that 196.608 MHz (S200) does not appear to be a supported electrical interface speed per Table 4-1.

5. Claims 20, 21, 24 - 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nimishakavi in view of IEEE P1394b in further view of Ryan (US Patent 6,169,501).

With regard to claim 20, Nimishakavi in view of IEEE P1394b teach the limitations of claim 19. Nimishakavi is silent with respect to a serial/parallel translator, 8B/10B decoder, and descrambler, but does state that his device is to be used for the sampling of data (see column 5, lines 16 – 20). Ryan teaches the addition of serial/parallel translator (see Figure 7) having a second data signal input (see Figure 7, 110), a synchronous pulse input (see figure 7, 112) and a parallel output (see Figure 7, 90), second data signal input being connected to first data signal input (see figure 7, 104, and figure 5, 10 where figure 5 is interpreted to be a representation of reference 104 of figure 7) for receiving data signal and synchronous pulse input being connected to synchronous pulse output (see figure 7, 104) for receiving synchronous pulse, and serial interface engine processing difference signal and synchronous pulse to generate parallel data for output on parallel output (see Figure 7, 90 and column 13, lines 22 – 39). Ryan fails to teach the 8B/10B decoder and the descrambler. The IEEE 1394b specification defines the use of 8B/10B encoding along with data scrambling (see section 4.4, and figure 10-2) and further discusses the need for reciprocal functions at the receive end (see page 141, last paragraph which would consist of serial-parallel conversion, 8B/10B decoder, and descrambler). Ryan further describes a control block, which includes counter and pulse generation circuitry. Ryan is silent on the details of his clock and pulse generation circuitry. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the device of Nimishakavi in view of IEEE 1394b with Ryan to create a configurable data rate receiver with a serial – parallel converter, 8B/10B decoder, and descrambler to create a flexible data receiver device. It is worth noting that Figure 10-2 of

IEEE 1394b specification defines the need for the serial to parallel conversion of data as the processing of data is shown as being performed on parallel data.

With regard to claim 21, Nimishakavi in view of USB in further view of Ryan teach the limitations of claim 20 above. Nimishakavi and Ryan are silent with respect to a packet receiver/transmitter having a parallel input. The IEEE 1394b specification defines the use of a packet receiver/transmitter having a parallel input (see figure 6-1, packet transmit/receive) that has a parallel input, parallel input being coupled to parallel output (see Figure 6-1, PMD, Port, packet transmit/receive, where this is interpreted to be parallel data) for receiving parallel data. It would have been obvious to one of ordinary skill in the art at the time of invention to use Nimishakavi and Ryan's combined device in an IEEE1394b system to provide to provide a configurable rate data receiver.

With regard to claim 24, Nimishakavi teaches a device having a synchronous pulse generator having a first data signal input (see Figure 4, RXD which is interpreted as being a recovered differential (difference) signal), a clock signal input (see Figure 4, DPLL Clock), a speed input (Figure 4, Count In) and a synchronous pulse output (see Figure 4, RxDPLL ClkOut where this signal is interpreted as being the same as SPG Out), data signal input being coupled to first output for receiving data signal see Figure 4, RXD which is interpreted as being a recovered differential (difference) signal), speed signal being adapted to receive a variable representative of communication link speed (see Figure 4, 40, 48) and clock signal input being adapted for receiving a clock signal (see column 4, lines 14 – 20, figure 3, 38), wherein synchronous pulse generator processes clock signal and data signal to generate a synchronous pulse used for extracting data from data signal (see figure 4, RxD, DPLL Clk, RxD Sync, 40, 52, RxDPLL ClkOut). Nimishakavi is silent with respect to a difference signal, serial/parallel translator, 8B/10B decoder, and descrambler, but does state that his device is

to be used for the sampling of data (see column 5, lines 16 – 20). Ryan teaches a serial to parallel converter (which is interpreted by examiner as providing equivalent functionality as applicant's SIE, see Figure 7, serial to parallel converter) having a second data (difference) signal input (see Figure 7, 110), a synchronous pulse input (see figure 7, 112) and a parallel output (see Figure 7, 90), second data (difference) signal input being connected to first data (difference) signal input for receiving data (difference) signal and synchronous pulse input (see Figure 7, 90, Out) being connected to synchronous pulse output (see figure 7, 104, Out) for receiving synchronous pulse (from figure 7, 104), and serial interface engine processing data (difference, figure 7, 110, 96, 90) signal and synchronous pulse to generate parallel data for output (see figure 7, Out(112)) on parallel output (see column 13, lines 22 – 39). Ryan further describes a control block, which includes counter and pulse generation circuitry. Ryan is silent on the details of his clock and pulse generation circuitry, .the generation of a difference signal representing a signal level difference between at least two data stream signals, the 8B/10B decoder and the descrambler. The IEEE 1394b specification defines the use of a differential signal for transmission of data (see page 45, section 4.4.2 2nd paragraph) and 8B/10B encoding along with data scrambling (see section 4.4, 10.2.5, 10.2.6, Figure 10-2) and further discusses the need for reciprocal functions at the receive end (see page 141, last paragraph which would consist of serial-parallel conversion, 8B/10B decoder, and descrambler). It would have been obvious to one of ordinary skill in the art at the time of invention to use Nimishakavi and Ryan's combined device in an IEEE 1394b system to provide to provide a configurable rate data receiver

With regard to claim 25, Nimishakavi in view of IEEE 1394b in further view of Ryan teach the limitations of claim 24 above. Nimishakavi and Ryan are silent on the use of connection manager having a toning input, a toning output and a bus speed output. IEEE 1394b

specification defines the use of connection manager having a toning input, a toning output and a bus speed output (see section 6.6, 6,6,1). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi and Ryan's combined device in an IEEE 1394b system to provide to provide a configurable data receiver.

With regard to claim 26, Nimishakavi in view of IEEE 1394b in further view of Ryan teach the limitations of claim 24 above with Nimishakavi teaching the additional limitation of synchronous pulse generator includes a speed register (see figure 4, 48 where count register is interpreted to store calculated speed value) for storing a speed value that corresponds with a communication speed of a serial bus.

With regard to claim 27, Nimishakavi in view of IEEE 1394b in further view of Ryan teach the limitations of claim 26 above. Ryan and Nimishakavi are silent with respect to communication link speed is a frequency of one of 98.304 MHz, 196.608 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz. IEEE 1394b teaches the additional limitation of communication link speed is a frequency of one of 98.304 MHz, 393.2 16 MHz, 786.432 MHz, 1 .572864 GHz and 3.145728 GHz (see page 46, table 4-1). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Nimishakavi's device in an IEEE 1394b system to provide to provide a configurable data receiver.

Other Cited Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Skergan (US Patent 6,226,345) teaches a configurable clock generator. Ryan (6,359,946), Miller (6,700,943), Barrow (5,809,091) teach data recovery with varying degrees of configurability. NPL documents provide further background information on IEEE-1394 specifications.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER

11/10/04